Amendments to the Specification

Please add the following paragraph to line 25, page 3, of the specification:

FIG. 2C illustrates another embodiment of the semiconductor device structure of **FIG. 2A**, in particular, a CMOS with P+ buried layer, plug and deep trench isolation structures.

Please add the following paragraph to line 1, page 10, of the specification:

FIG. 2C shows a CMOS with a low resistive path barrier and deep trench isolation according to alternative embodiments of the invention. The structure depicted in **FIG. 2C** is similar to the structure of **FIG. 2B** except that the buried layer **203** is a P+ buried layer instead of an N+ buried layer, the plug **205** is a P+ plug instead of an N+ plug, and the substrate **111** is an N type substrate rather than a P type substrate.